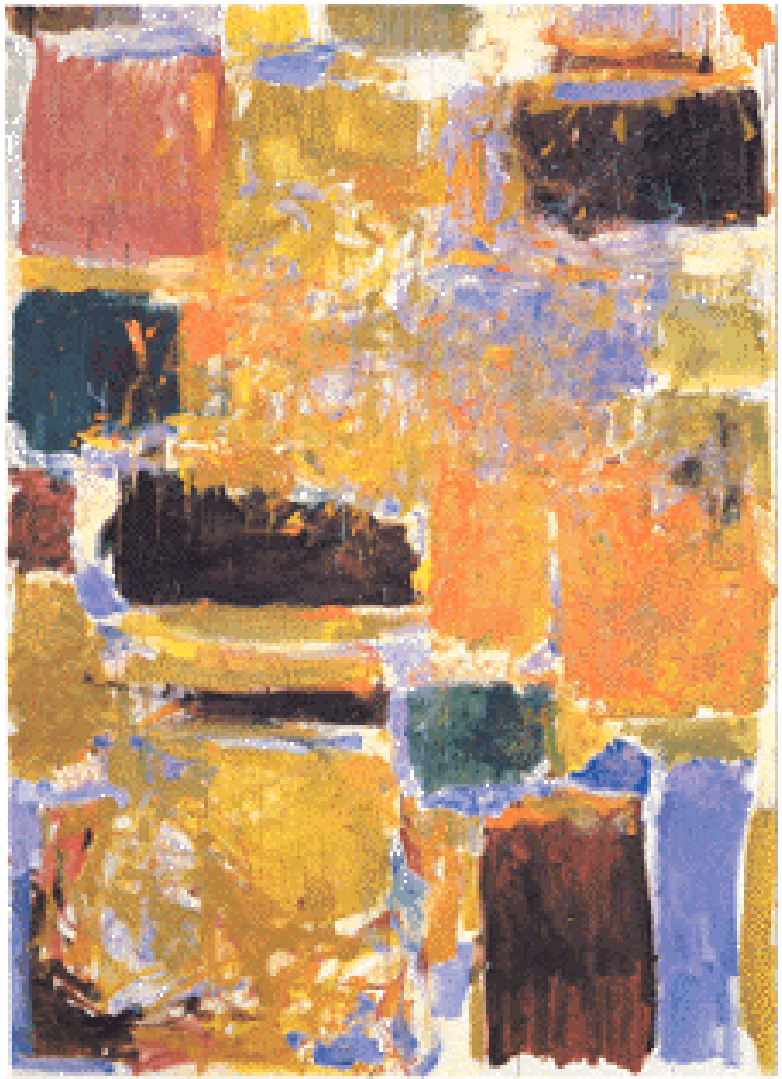
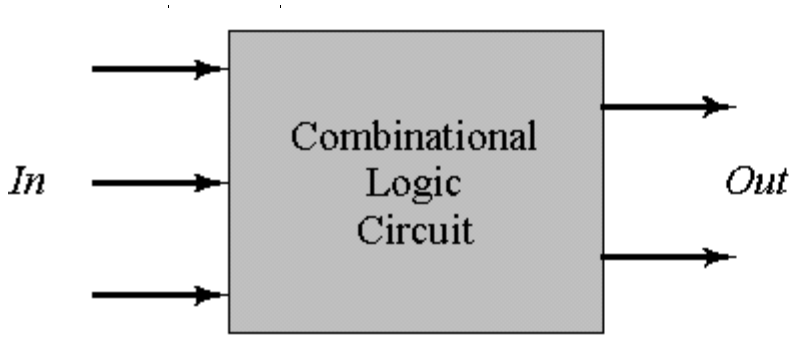
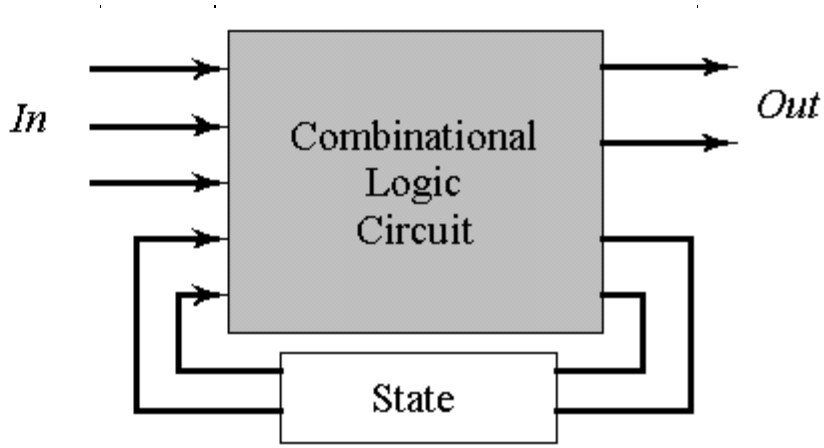


Designing Combinational Logic Circuits

Combinational vs. Sequential Logic





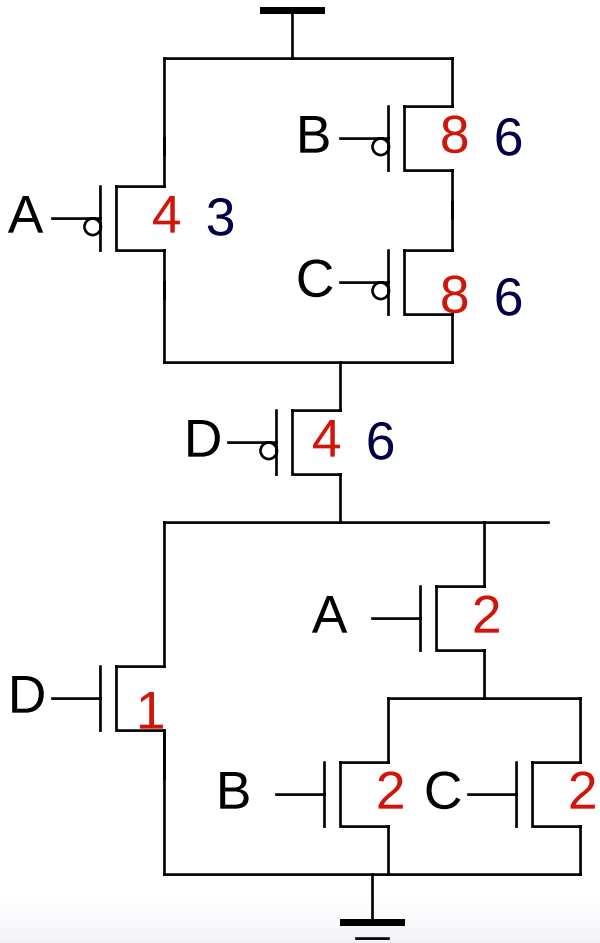
Combinational

Sequential

Output = *f*(*In*)

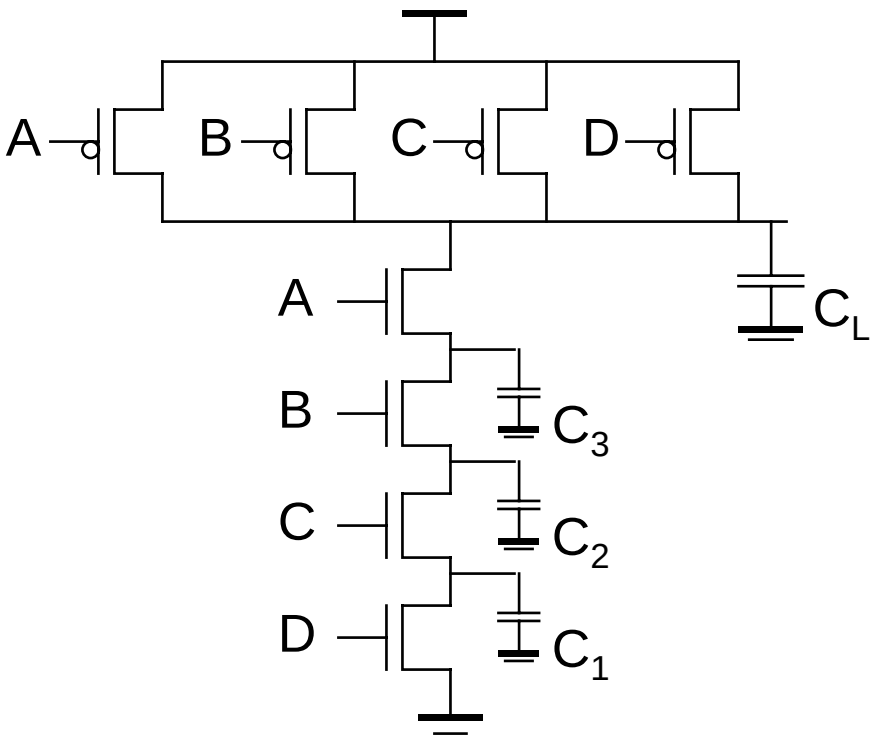
Output = *f*(*In*, *Previous In*)

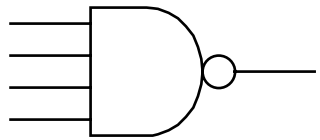
Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$

Fan-In Considerations





Distributed RC model (Elmore delay), assuming all NMOS devices of equal size

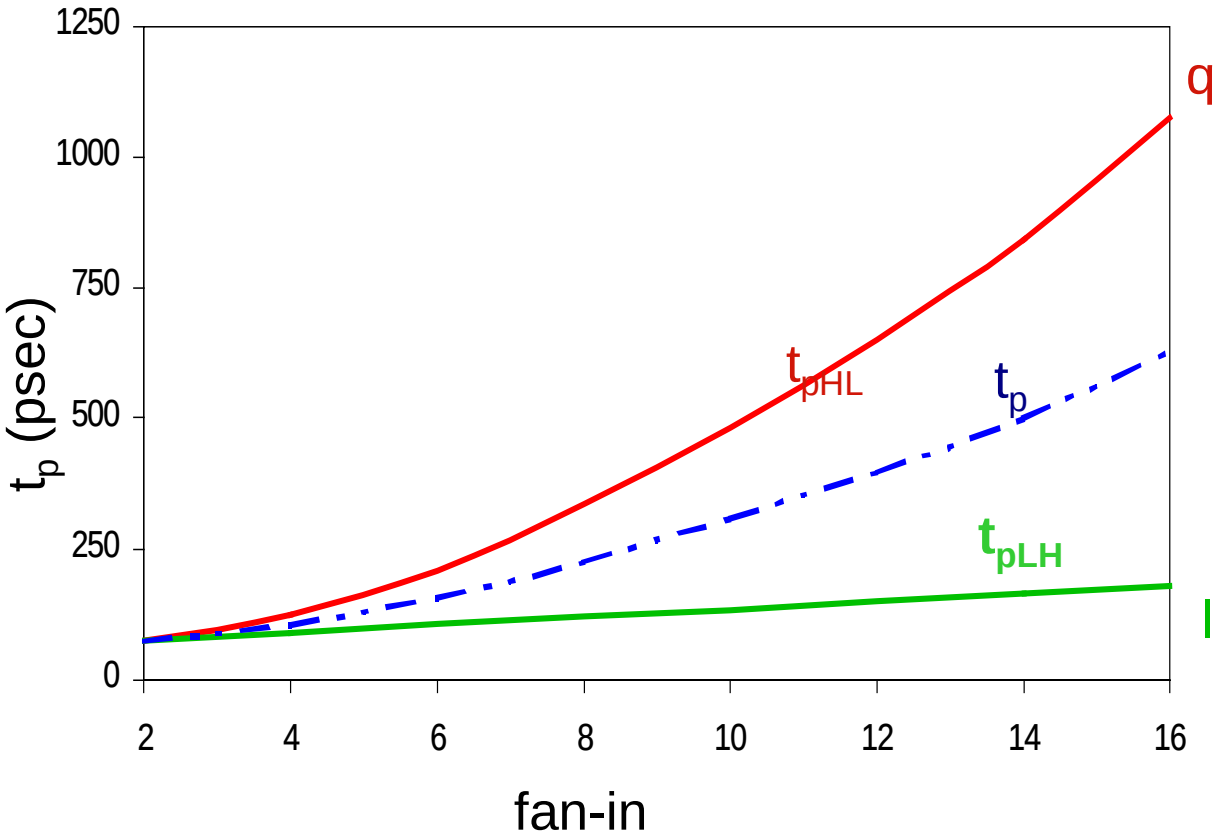
$t_{pHL} = 0.69\, R_{eqn}(C_1+2C_2+3C_3+4C_L)$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

$$t_{pHL} = 0.69\left[R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + (R_1+R_2+R_3+R_4)C_L\right]$$

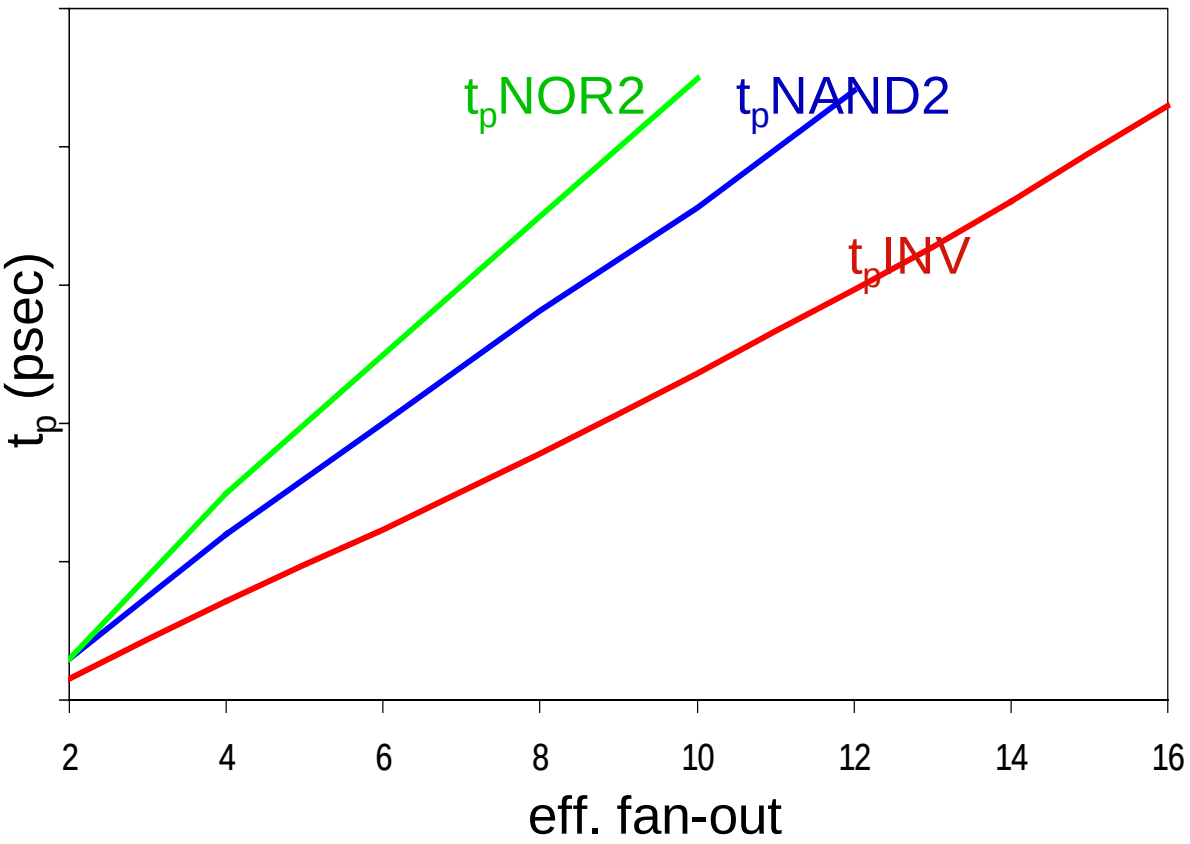
t_p of CMOS NAND as a Function of Fan-In

(Assuming a fixed fan out of one inverter)



Gates with a fan-in greater than 4 should be avoided.

t_p as a Function of Fan-Out

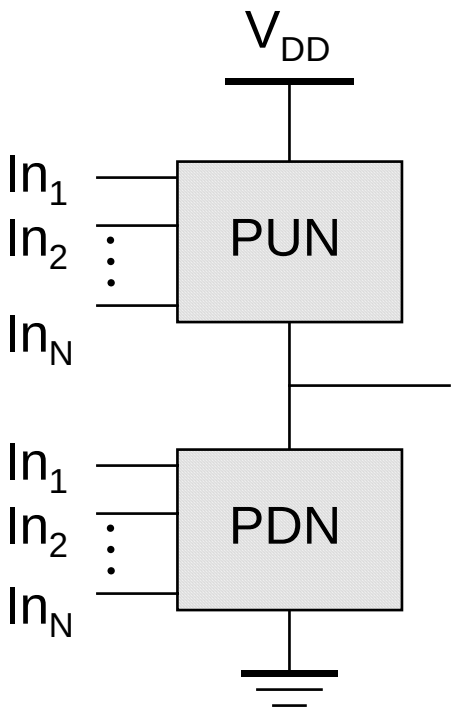


All gates have the same drive current.

Slope is a function of "driving strength"

Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

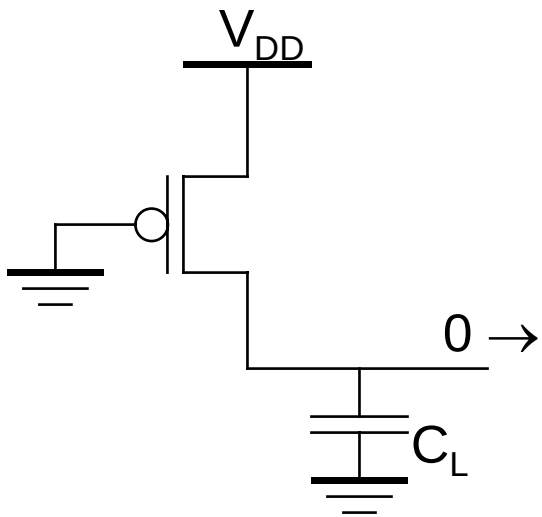
NMOS transistors only

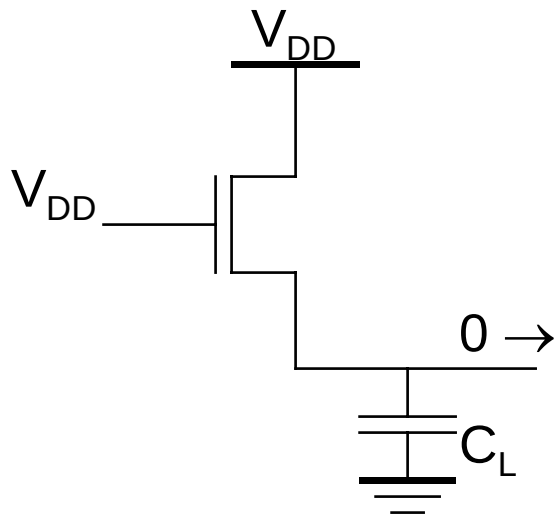
PUN and PDN are dual logic networks

One and only one of the networks is conducting in steady state

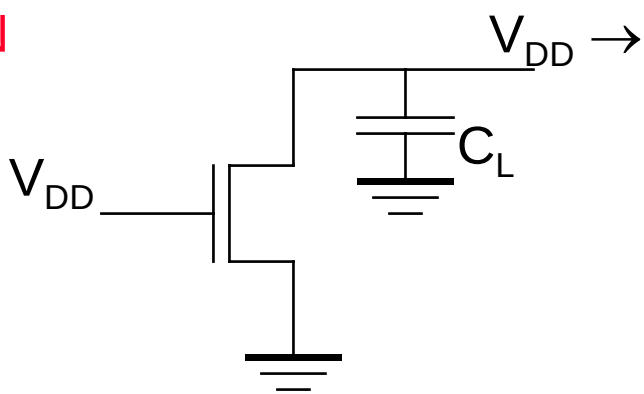
Threshold Drops

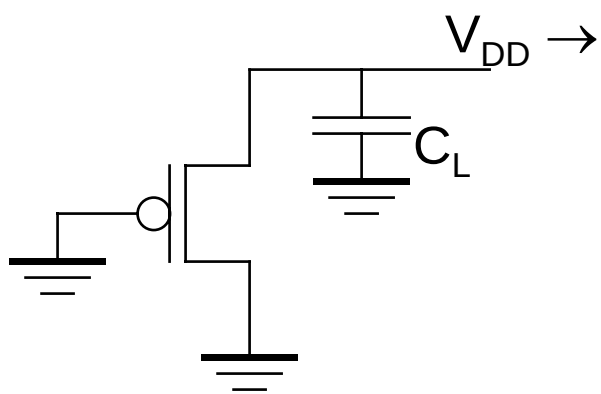
PUN



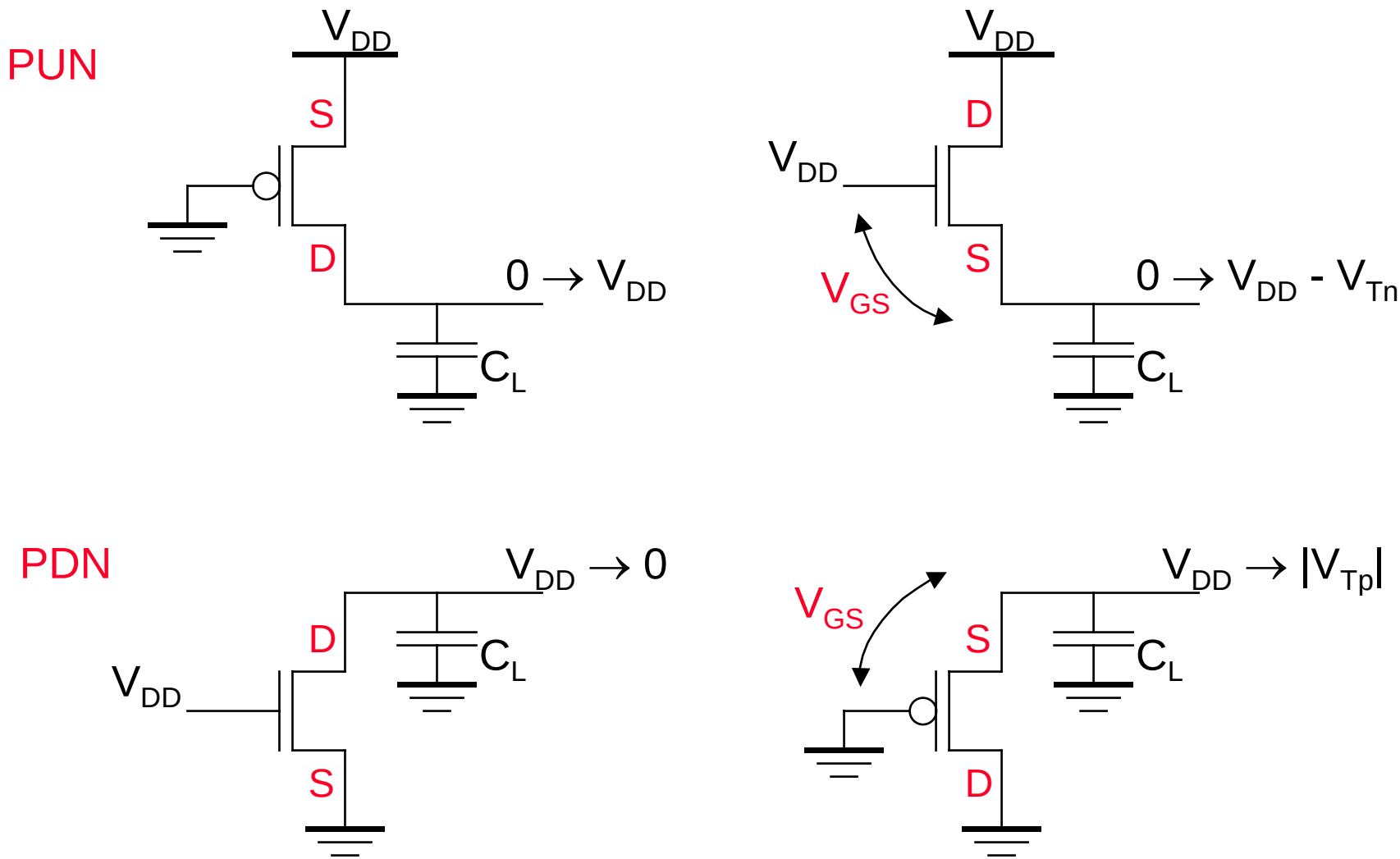


PDN





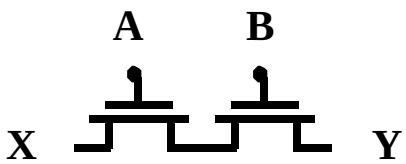
Threshold Drops



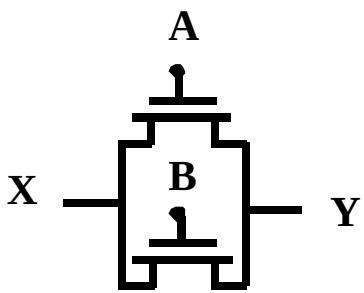
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

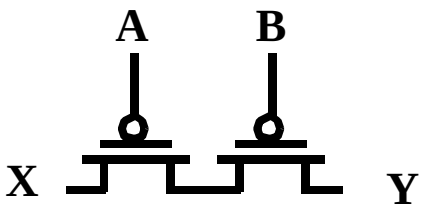


Y = X if A OR B

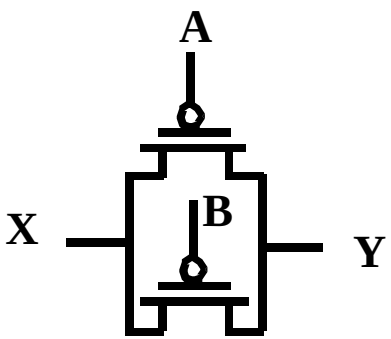
NMOS Transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

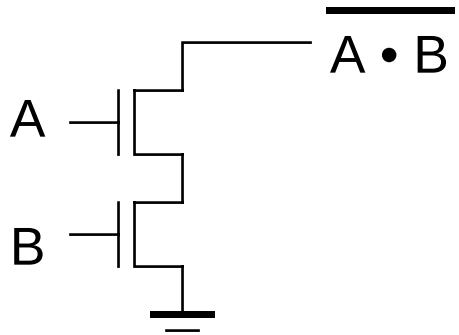


$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

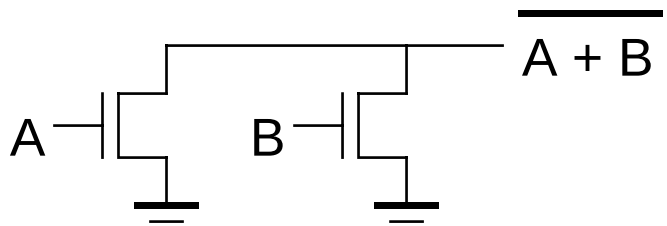
PMOS Transistors pass a “strong” 1 but a “weak” 0

Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

- PUN and PDN are dual networks
  - DeMorgan's theorems

$$\overline{A + B} = \overline{A} \bullet \overline{B}$$

$$\overline{A \bullet B} = \overline{A} + \overline{B}$$

  - a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- Complementary gate is naturally inverting (NAND, NOR, XNOR)
- Number of transistors for an N-input logic gate is 2N

Complementary CMOS Logic Style

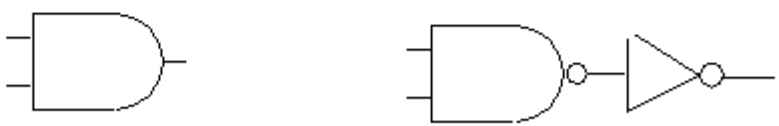
- **PUN is the DUAL of PDN**

  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

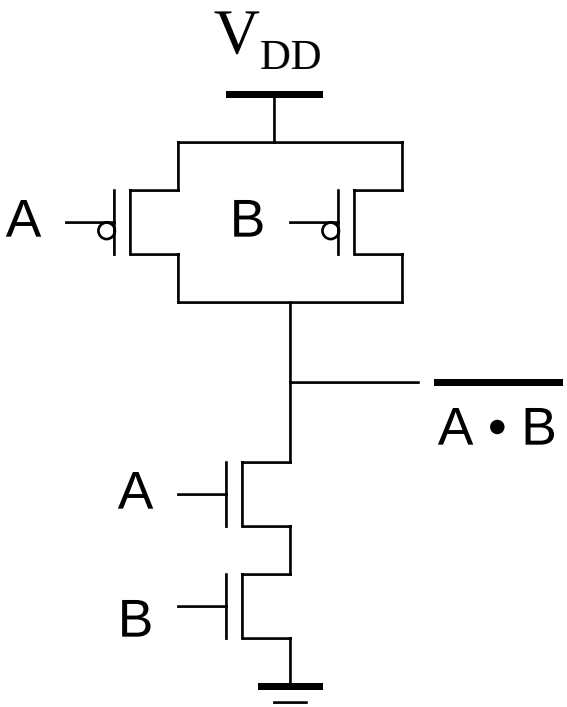
$$\overline{AB} = \bar{A} + \bar{B}$$

- **The complementary gate is inverting**

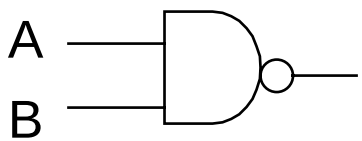


AND = NAND + INV

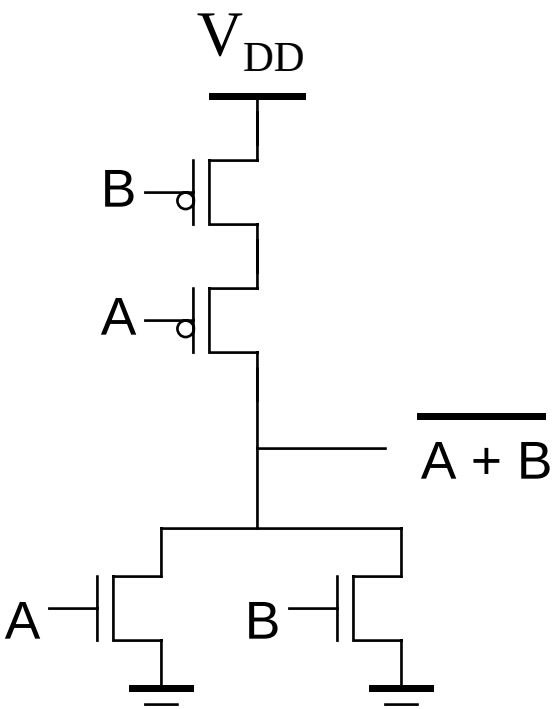
CMOS NAND



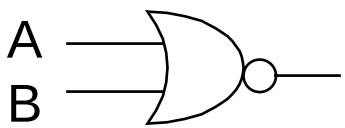
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



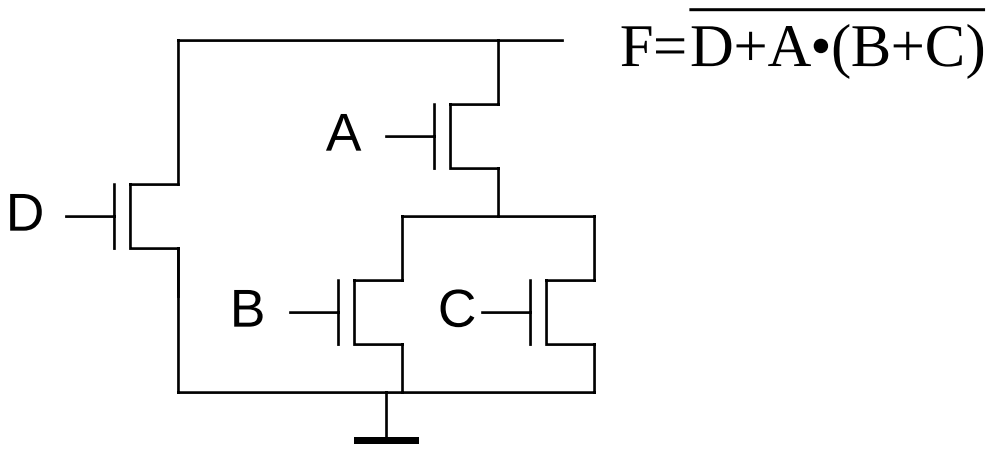
CMOS NOR



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



Complex CMOS Gate



Complex CMOS Gate